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Space time coding transmitter based on VHDL

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بِسْمِ اللّٰهِ الرَّحمَن الرَّحِيمِ

((وَ قُل رَّبِّ زِدْنى عِلْماً))

﴿ ١١٤ ﴾

صَدَقَ اللّٰهُ العَظِيم

بسم الله الرحمن الرحيم

(قَالُواْ سُبْحَانَكَ لاَ عِلْمَ لَنَا إِلاَّ مَا عَلَّمْتَنَا إِنَّكَ أَنتَ الْعَلِيمُ الْحَكِيمُ)

صدق الله العظيم

آية (٣٢) من سورة البقرة

Acknowledgment

First of all, I give my thanks forever to Allah who enabled me to complete this work.

I take this opportunity to express my sincere gratitude towards my Supervisor Adham Hadi Saleh for his advices, encouragement and cooperation. He has been a source of inspiration and has provided consistent succor and valuable suggestions throughout this project without which this work would not have been possible.

I would like to express my heart-felt gratitude to my parents for their encouragement and support without which I would not have come so far.

I am very grateful to my mother , my father, brothers, my friends and all who supported me.

Examination committee certification

We certify that we have read this thesis entitled "**Space time coding transmitter based on VHDL** ". We as an examining committee examined the student "**Bahaa Al-deen Mohammed Mahmood and Amna Hashim Abass** " and found that the thesis meet the standard for the degree of Bachelor in Electronic Engineering.

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Date**: / / 2016**

(Chairman)

Signature:

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Date**: / / 2016**

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Supervisor Certification

I certify that this thesis entitled **"Space time coding transmitter based on VHDL "** was prepared under my supervision at the Department of Electrical Power & Machines Engineering, University of Diyala in partial fulfillment of the requirements for the degree of Bachelor of Science In Electronic Engineering

Signature:

Name**:**

Date: / / 2016

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Terminology :

MIMO	multiple input multiple output
STC	space time coding
VHDL	VHSIC Hardware Description Language
BER	Bit error rates
SC	Selection combining
MRC	Maximal ratio combining
EGC	Equal gain combining
MRT	Maximal ratio transmission
STBC	Space time block coding
CDMA	Code division multiple access
OFDM	Orthogonal frequency division multiplexing
MISO	Multiple input single output
QPSK	Q_ Phase shift keying
DFF	D-flip –flops
SISO	Single input single output
SIMO	Single input multiple output
VHSIC	Very high speed integrated circuits
ASIC	Application specific integrated circuits
ISE	Integrated software environment

Figures :

Abstract

The use of multiple transmit and receive antennas (MIMO system) is widely accepted in recent years, as a promising technology for future wireless communication, due to its ability to achieve higher data rates without increasing the transmission power and bandwidth, in addition to its ability to improve system reliability through increasing diversity. MIMO system is associated with coding techniques which have been proposed as a way to fulfill the demand for increased the capacity and the performance of wireless communication systems. MIMO system are particularly attractive because they do not require any additional transmission bandwidth. The implementation demonstrates the space-time code in a baseband system with two transmitted antennas and(two received antennas in one system,) with the encoding and decoding algorithms using (VHDL).A developed mobile channel model has been designed using VHDL to connect the transmitter antennas with the received antennas.

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Chapter One

General Introduction

1.1 Introduction:

Became for wireless communication essential role in person life entered community. Wireless system designers are facing a number of challenges. These include the limited availability of the radio frequency spectrum and a complex space–time varying wireless environment. In addition, there is an increasing demand for higher data rates, better quality of service, and higher network capacity. In recent years, Multiple-Input Multiple-Output (MIMO) systems have emerged as a most promising technology in these measures. The core idea behind MIMO is that signals sampled in the spatial domain at both ends are combined is such a way that they either create effective multiple parallel spatial data pipes (therefore increasing the data rate), and/or add diversity to improve the quality (bit error rate) of the communication. Clearly, the benefits from multiple antennas arise from the use of a new dimension – space. Hence, because the spatial dimension comes as a complement to time (the natural dimension of digital communication data), MIMO technology is also known as 'space–time' wireless or 'smart' antennas [1].

The communications systems with multiple transmit and receive antennas (*MIMO*) present a better performance on two different angles, the diversity and the multiplexing. The diversity gain is responsible for the improvement in the quality of communication link and is obtained through the use of Space Time Coding (*STC*). To obtain space diversity gain must be used multiple transmit antennas and at least one receive antenna. The space multiplexing needs in the reception a number of antennas bigger or equal of the transmission, exploring the parallelism of channels to increase the transmission rate. The first excellent work in the space-time coding subject was

presented for Alamouti, Slavish . In his work the transmission necessarily occurs through two antennas, with one or more antennas in the reception [2].

1.2 Literature survey:

S. M. Alamouti , 1998 [8] presented a simple two-branch transmit diversity scheme. Using two transmit antennas and one receive antenna, the scheme provides the same diversity order as Maximal Ratio Combining (MRC) at the receiver, with one transmit antenna, and two receive antennas. The new scheme does not require any bandwidth expansion, any feedback from the receiver to the transmitter, and its computation complexity is similar to MRC.

Wittneben, 1993 [11] proposed one of the earliest form of spatial transmit diversity, called delay diversity scheme, where a signal is transmitted from one antenna, then delayed one time slot, and transmitted from the other antenna.

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Wireless stepper motor controller designed using Very High Speed Integrated Circuit Hardware Description Language (VHDL) and is implemented on SPARATAN Field Programmable Gate Array (FPGA). The proposed motor controller is controlled by using Pulse Width Modulation Technique (PWM) thus giving the very high precision. Due to high torque of stepper motor it is capable of handling the big industrial automation system. In this system GUI will be designed using LABVIEW to give the control parameter to the wireless connected stepper motor. Same system can also be used in the mobile robot, functioning in the hazardous area and can be very well equipped with the nuclear reactor to control the movement of control rod. One of the

best use is to track solar energy because the resolution of stepper motor will be highly increased i.e. 0.915˚.

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They discuss logic circuit designs using the circuit model of three-state quantum dot gate field effect transistors (QDGFETs). QDGFETs produce one intermediate state between the two normal stable ON and OFF states due to a change in the threshold voltage over this range. We have developed circuit model which has intermediate state. Various logic can be implemented using QDGFETs. In this paper, we have discussed the designs of various three-state QDGFET combinational circuits like decoder, and comparator. Increased number of states in three-state QDGFETs will increase the number of bit-handling capability of this device and will help us to handle more number of bits at a time with less circuit elements.

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The growing demand for high density VLSI circuits the leakage current on the oxide thickness is becoming a major challenge in deep-sub-micron CMOS technology. In deep submicron technologies, leakage power becomes a key for a low power design due to its ever increasing proportion in chip‟s total power consumption. Motivated by emerging battery-operated application on one hand and shrinking technology of deep sub micron on the other hand, leakage power dissipation is playing a significant role in the total power dissipation as threshold voltage becomes low. Due to the trade-off between power, area and performance, various efforts have been done. This work is

also based to reduce the power dissipation of the VLSI circuits with the performance up to the acceptable level. Here we proposed Novel SRAM architecture called IP-SRAM with separate write sub-cell and read sub-cell. In this paper we designed the total 8 bit SRAM architecture with newly proposed techniques and compare this one with conventional SRAM architecture and we observed that the total power consumption is reduced. Here the total architecture was designed with 180nm technology.

K.V.GANESH*,D.SRI HARI,M.HEMA*****

The design and implementation of a programmable cyclic redundancy check (CRC) computation circuit architecture, suitable for deployment in network related system-on-chips (SoCs) is presented. The architecture has been designed to be field reprogrammable so that it is fully flexible in terms of the polynomial deployed and the input port width. The circuit includes an embedded configuration controller that has a low reconfiguration time and hardware cost. The circuit has been synthesised and mapped to 130-nm UMC standard cell ASIC technology and is capable of supporting line speeds of 5Gb/s.

1.3 Project objectives:

- Identify the software of VHDL and use it to design and simulation of space time code transmitter.

1.4 Theses Out lines:

- In chapter two will explain the diversity and space time coding.
- In chapter three will explain the VHDL language.
- In chapter four will explain the work and the result of the experiments.
- In chapter five will introduce conclusion and future work.

Chapter Two

Diversity

2.1 Introduction:

This Chapter Describe Multipath Channel Causes Significant Impairments To The Signal Quality In Mobile Radio Communication Systems. As Signals Travel Between The Transmitter And Receiver, They Get Reflected, Scattered, And Diffracted. In Addition, User's Mobility Gives Rise To Doppler Shift In The Carrier Frequency. As A Result, Those Signals Experience Fading (I.E., They Fluctuate In Their Strength). When The Signal Power Drops Significantly, The Channel Is Said To Be In Fade. This Gives Rise To High Bit Error Rates (BER) [4,3].

To Combat The Impact Of Fading On The Error Rate, Diversity Techniques Are Usually Employed Which Is Applied To Multi-Antenna Systems (The Use Of Multiple Antennas At The Transmitter And/or The Receiver) [7,13]. The Principle Of Diversity Is To Provide The Receiver With Multiple Versions Of The Same Transmitted Signal. Each Of These Versions Is Defined As A Diversity Branch. If These Versions Are Affected By Independent Fading Conditions, The Probability That All Branches A In Fade At The Same Time Is Reduced Dramatically [7].

In A Wireless Communications System, This Results In An Improvement In The Required SNR Or E_s/N_o Is Necessary To Achieve A Given Quality Of Service In Terms Bit Error Rate (BER).[9]

In This Chapter, Types Of Diversity Techniques Will Be Introduced, Then, Receive Diversity Combining Techniques Which Are, Selection Combining (SC), Maximal

Ratio Combining (MRC) And Equal Gain Combining (EGC) Will Be Studied And Analyzed. Finally, Transmit Diversity Combining Techniques Such As, Maximal Ratio Transmission (MRT) And Space -Time Block Codes (STBC) Will Be Presented.

2.2 Types of Diversity Techniques

Diversity involves providing replicas of the transmitted signal over time ,frequency, or space. Therefore, three types of diversity schemes can be found in wireless communications [3].

2.2.1 Time diversity: In this case, replicas of the transmitted signal are provided across time by a combination of channel coding and time interleaving strategies. The key requirement here for this form of diversity to be effective is that the channel must provide sufficient variations in time. It is applicable in cases where the coherence time of the channel is small compared with the desired interleaving symbol duration. In such an event, it is assured that the interleaved symbol is independent of the previous symbol. This makes it a completely new replica of the original symbol [3].

2.2.2 Frequency diversity: This type of diversity provides replicas of the original signal in the frequency domain. This is applicable in cases where the coherence bandwidth of the channel is small compared with the bandwidth of the signal [3]. This will assure that different parts of the relevant spectrum will suffer independent fades. Frequency diversity can be utilized through spread spectrum techniques or through interleaving techniques in combination with multicarrier modulation. For example, Code-Division Multiple- Access (CDMA) systems such as the Direct-Sequence CDMA and Frequency-Hopping CDMA as well as the Orthogonal Frequency-Division Multiplexing (OFDM) systems are based on frequency diversity, however frequency diversity techniques use much more expensive frequency spectrum and require a separate transmitter for each carrier [10,8].

2.2.3 Space diversity: Recently, systems using multiple antennas at transmitter and/or receiver gained much interest [14]. The spatial separation between the multiple antennas is chosen so that the diversity branches experience uncorrelated fading [6]. Unlike time and frequency diversity, space diversity does not induce any loss in bandwidth efficiency. This property is very attractive for high data rate wireless communications [11]. In space, various combining techniques, i.e., Maximum-Ratio Combining (MRC), Equal Gain Combining (EGC) and Selection Combining (SC), may be used at the receiver. Space-time codes which exploit diversity across space and time can also be used at the transmitter side [3].The diversity type which utilized in this thesis is the spatial diversity and all the combining techniques mentioned above will be examined in this chapter**.** In the category of spatial diversity, there are two more types of diversity that must be considered:

2.2.3.1 Polarization diversity: In this type of diversity, horizontal and vertical polarization signals are transmitted by two different polarized antennas and received correspondingly by two different polarized antennas at the receiver. The benefit of different polarizations is to ensure that there is no correlation between the data streams [11]. In addition to that, the two polarization antennas can be installed at the same place and no worry has to be taken about the antenna separation. However, polarization diversity can achieve only two branches of diversity. The drawback of this scheme is that a 3 dB extra power has to be transmitted because the transmitted signal must be fed to both polarized antennas at the transmitter [13].

2.2.3.2 Angle diversity: This applies at carrier frequencies in excess of 10GHz. In this case, as the transmitted signals are highly scattered in space, the received signals from different directions are independent to each other. Thus, two or more directional antennas can be pointed in different directions at the receiver site to provide uncorrelated replicas of the transmitted signals [11].

2.3 Space-time Block Codes:

2.3.1 Introduction:

In recent years, space-time coding techniques have received much interest. The concept of space-time coding has arisen from diversity techniques using smart antennas. By using data coding and signal processing at both sides of transmitter and receiver, space-time coding now is more effective than traditional diversity techniques [15], [16], [17], and [18]. Mostly, traditional diversity techniques are receive diversities. The problem with receive diversity for mobile communications is that the receive antennas had to be sufficiently apart so that the signals received at each antenna undergoes independent fade. Because of that, it is very costly to have more than one antenna in the mobile unit because they meant to be small in size and light in weight. Therefore, the use of transmit diversity in base stations appears to be an attractive method, as more complex base stations can be allowed [19], [20], [21] and [22]. Base stations have the advantage of using both transmit and receive diversities when they communicate with each other, the case of multiple input multiple output (MIMO) channels. Moreover, transmit diversity could also be used when base stations need to transmit information to the mobile units which forms the channel of multiple input single output (MISO).

2.3.2 Alamouti Space-Time Code:

Alamouti scheme is the first space-time block code scheme that provides full transmit diversity for systems with two transmit and one receive antennas [24]. It is a unique scheme in that it is the only space-time block code with an T n x T n complex transmission matrix to achieve the full rate of one [23]. In this section, we present Alamouti' transmit diversity technique in details, which includes the encoding and decoding algorithms. In addition to that, the performance of the scheme is discussed and analyzed using the simulations results .

2.3.3 Alamouti Encoding:

At the transmitter side, a block of two symbols are taken from the source data and sent to the modulator. After that, Alamouti space-time encoder takes the two modulated symbols, in this case called and at a time and creates encoding matrix where the symbols and are mapped to two transmit antennas in two transmit times as defined in the following:

$$S = \begin{bmatrix} s_1 & s_2 \\ -s_2^* & s_1^* \end{bmatrix} \qquad (2.1)$$

where the symbol * represents the complex conjugate. Therefore,S1* is the complex conjugate S1 of . The encoder outputs are transmitted in two consecutive transmission periods from the two transmit antennas. In the first transmission period, the signal S1 is transmitted from antenna one and the signal S2 is transmitted from antenna two, simultaneously. In the second transmission period, the signal is -S2 * transmitted from antenna one and the signal S1 * is transmitted from antenna two. The block diagram of the transmitter side using Alamouti space-time encoder is shown in Figure(2.1).

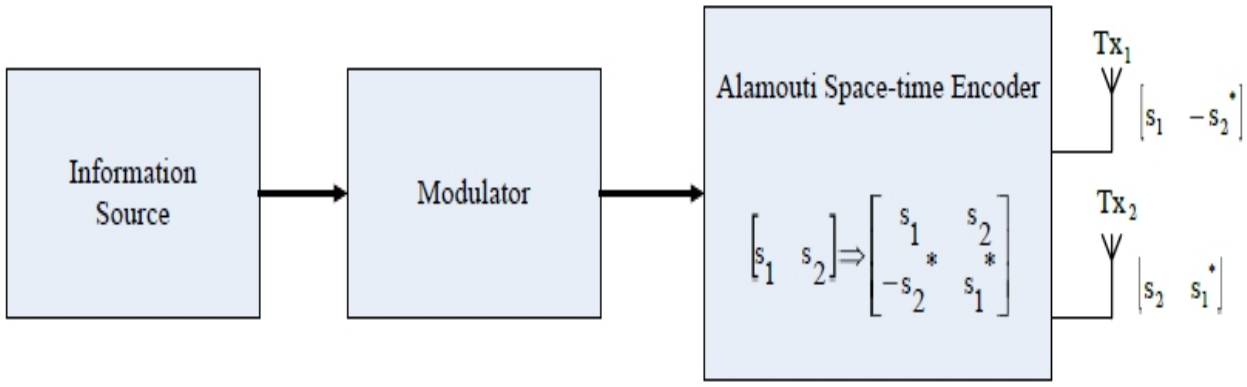


Figure (2.1): Alamouti space-time encoder diagram

Table (2.1): Encoding and mapping for two transmit antennas using complex signals.

	Tx_1	Tx_2
t	s_1	s_2
t+T	$-s_2^*$	s_1^*

where t represents the transmission symbol period, Tx1 and Tx2 are the first and second transmit antennas. The transmit sequence from antennas one and two denoted by s1 and s2 are encoded in both space and time domains.

$$s^1 = [s_1 \quad -s_2^*]$$
$$s^2 = [s_2 \quad s_1^*] \qquad (2.2)$$

The inner product of S1 and S2 is equal to zero. This confirms the orthogonality of the Alamouti space-time scheme.

2.3.4 Alamouti Transmitter:

Figure(2.2) shows the block diagram of Alamouti Transmitter which consist of three sub-blocks. These sub-blocks are the serial-to-parallel converter, QPSK modulator and Alamouti encoder. All these sub-block are made up of several blocks ,which will be discussed further later in this section. Data in is the serial binary bits input data which are being fed into the Alamouti transmitter design. The Alamouti transmitter design, manipulates these binary bits in such a manner that it follows the Alamouti transmit diversity technique to produce outputs at two transmit antenna.

At this point, please take note that the there is an assumption that the fading and inputs are constant for the duration of the encoding process, two consecutive symbols.

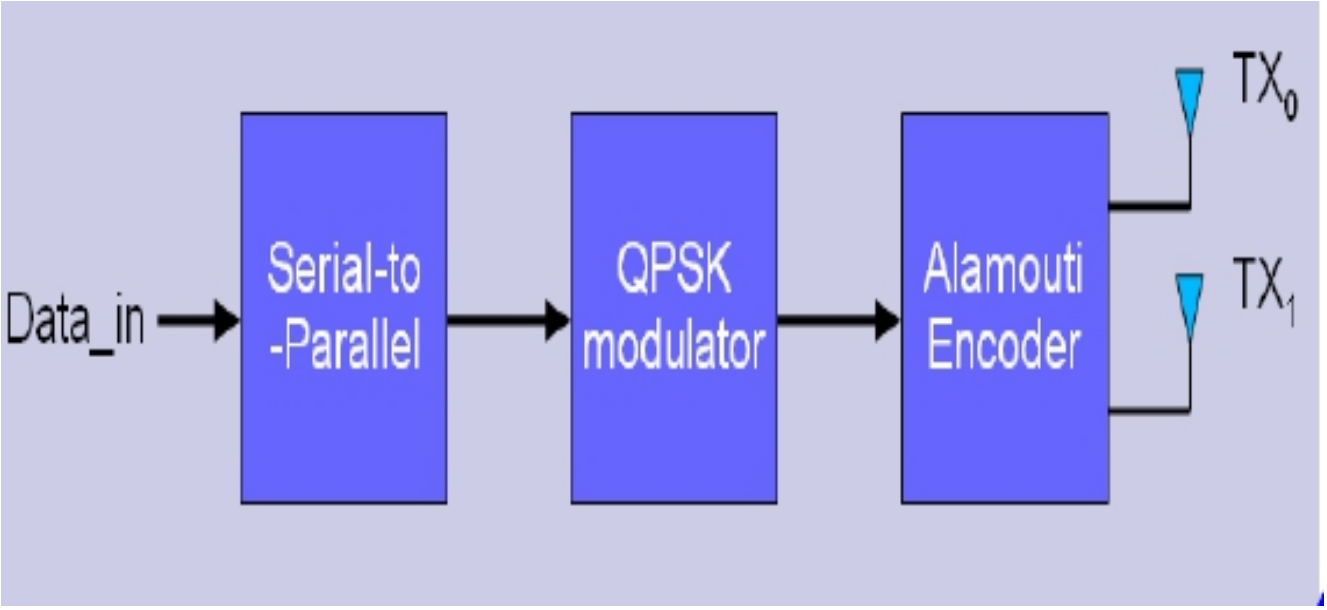


Figure (2.2): Block Diagram of Alamouti Transmitter

First, the Data_in information bits which are being fed in to the design in series are being converted into parallel data by the serial to parallel converter block performing the conversion. The output from this block is fed into the QPSK modulator which maps the data and produce symbols of complex numbers. There is an assumption that these numbers are integers. These symbols are passed to the Alamouti encoder which performs the negation of either the real or the imaginary part of the modulated symbol. The output of the encoding process is two streams of modulated symbols. Each stream can be fed to identical transmit chains each driving a separate antenna.

2.3.4.1 Serial-to-Parallel Converter:

A serial to parallel converter is a typical application of shift register. It consists of sending out a block of data parallel. The schematic of a serial to parallel converter is shown in Figure 2.3. It has a serial data input (Data_in), enable input (en), clock input (clk), reset input (rst), parallel data outputs (out a, out b, out c,out d) and a control signal output (Valid 4). The pin description of each input/output port is given in Table (2.2).

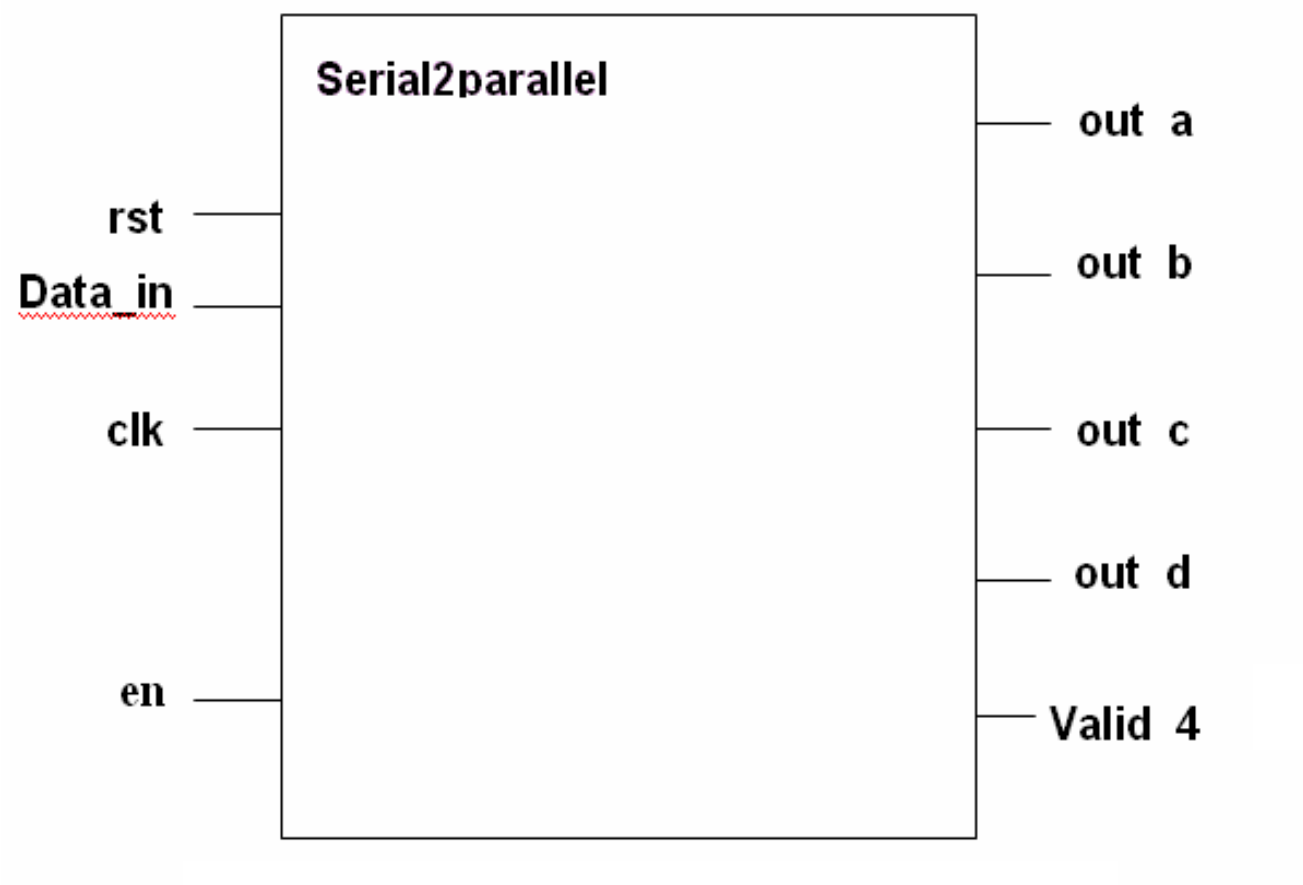


Figure (2.3): Serial-to-parallel

Signal	Direction	Size	Description
clk	Input	1	Clock signal that clocks all internal serial to parallel engine component.
en	Input	1	Active-high enable input. When de-asserted, the serial to parallel is disabled.
rst	Input	1	Reset signal that resets the serial to parallel when asserted.
Data_in	Input	1	Input data represented in binary bit stream.
out_A	Output	1	Output data represented in binary bit.
out_B	Output	1	Output data represented in binary bit.
out_C	Output	1	Output data represented in binary bit.
out_D	Output	1	Output data represented in binary bit.
Valid_4	Output	1	Output control signal, which is enabled when the conversion is completed.

Table (2.2): Input-Output pin description of serial-t-parallel module

Figure(2.4) shows the internal part of the serial-to-parallel converter. It is obvious here that the serial-to-parallel converter is made up of a shift register(Shift_reg), two control units (double_clk) and five D flip-flops (DFF). Each of these sub-blocks plays a different role in order to manipulate input data to perform the conversion of serial data to parallel data of 4 bits.

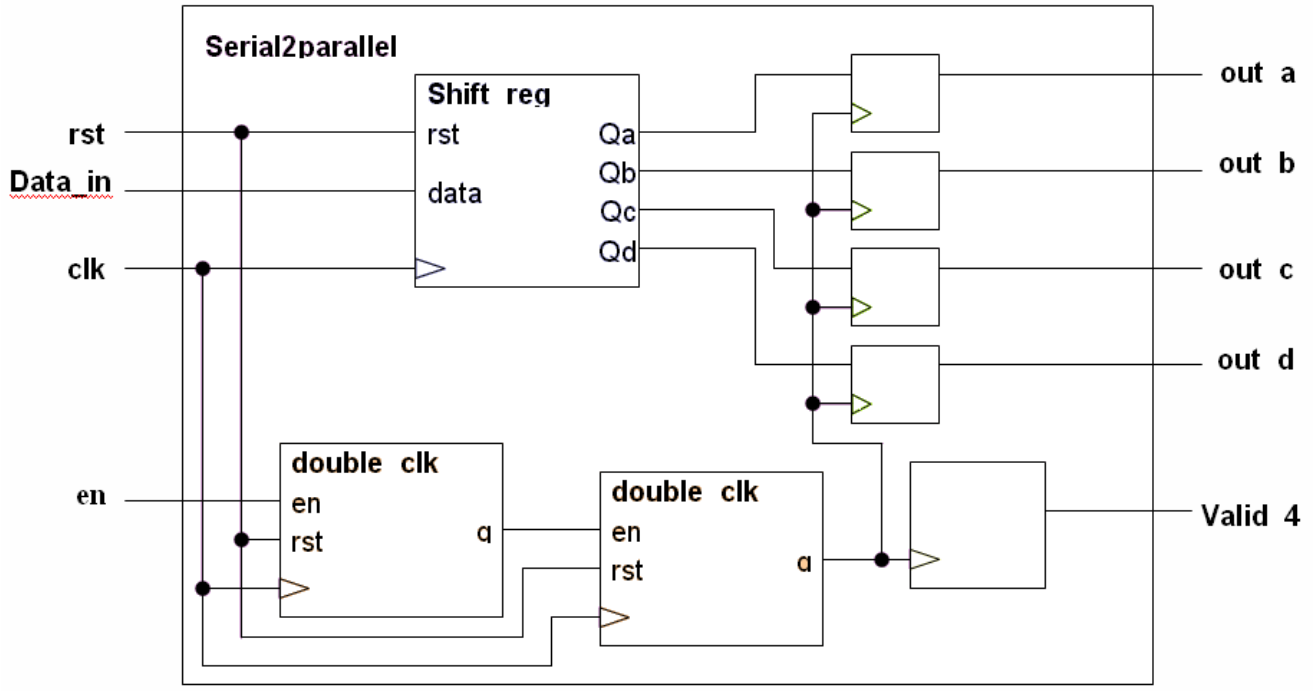


Figure (2.4): Internal part of the Serial-to-Parallel Converter

2.3.4.2 QPSK Modulator:

The QPSK modulator maps the groups of 2 bits of the input into QPSK constellations. The QPSK modulator (QPSK_mod) circuit is as shown in Figure (2.5) has reset input (rst), clock input (clk), enable input (en), reset input (rst_n), two bit input data (inp), eight bit real part of complex number output (q_out) and eight bit imaginary part of complex number output. The resulting output waveform of the QPSK modulator is shown in Figure (2.6). The modulator circuit consists of two parts which are the QPSK constellation (qpsk_const) and a QPSK control unit (ctrl_unit_qpsk) as shown in Figure (2.7).

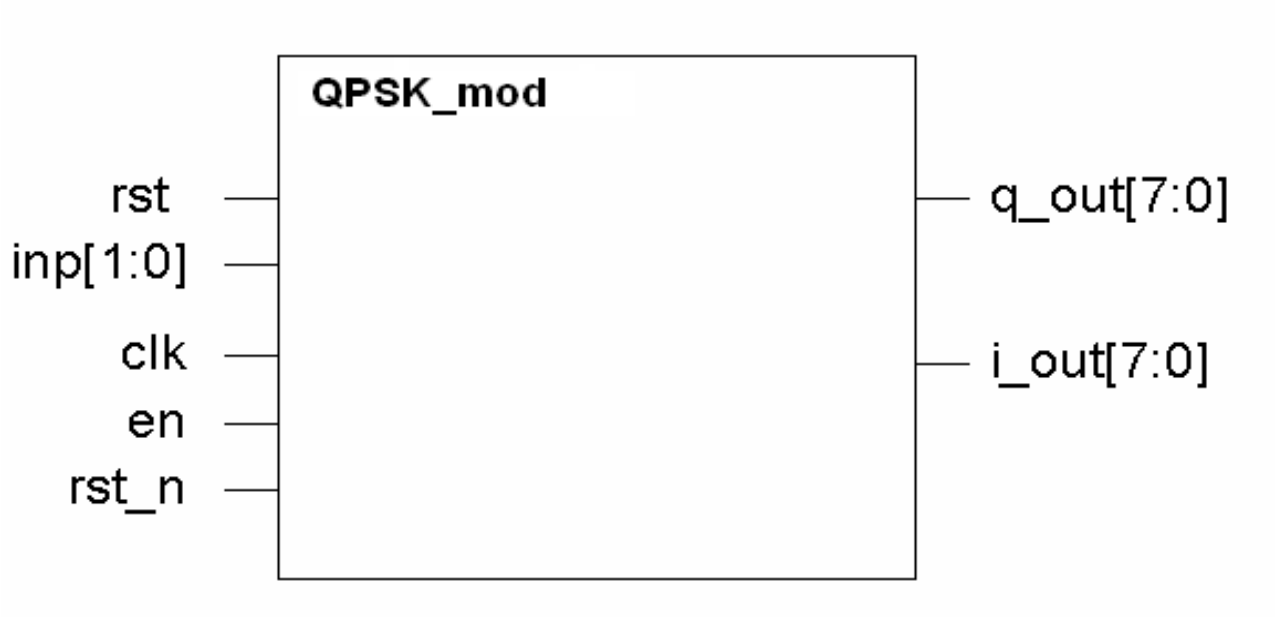


Figure (2.5): QPSK modulator

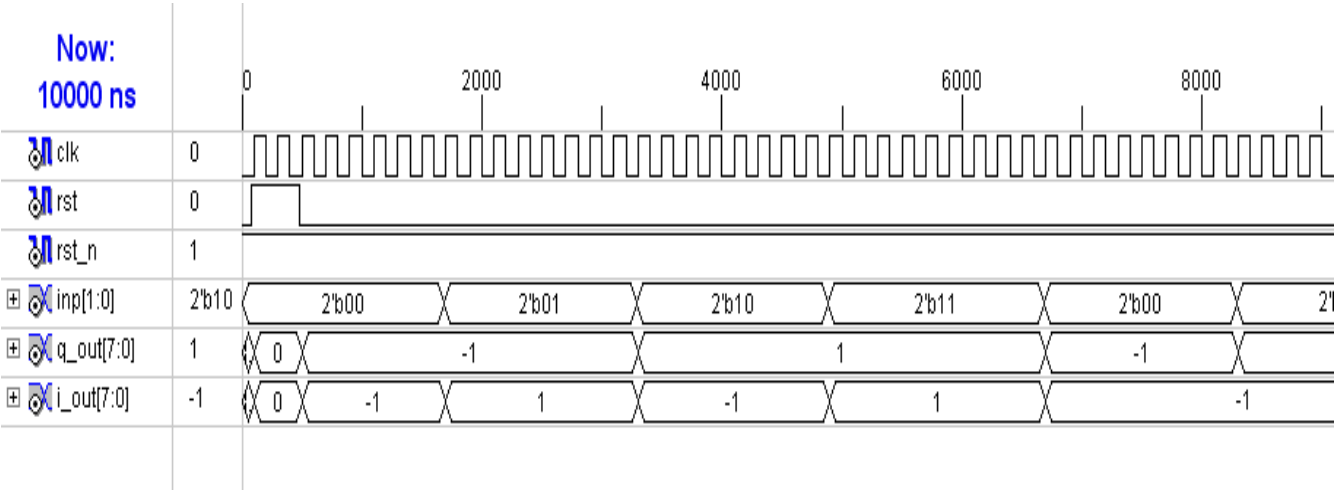


Figure (2.6): Output waveform of QPSK_mod

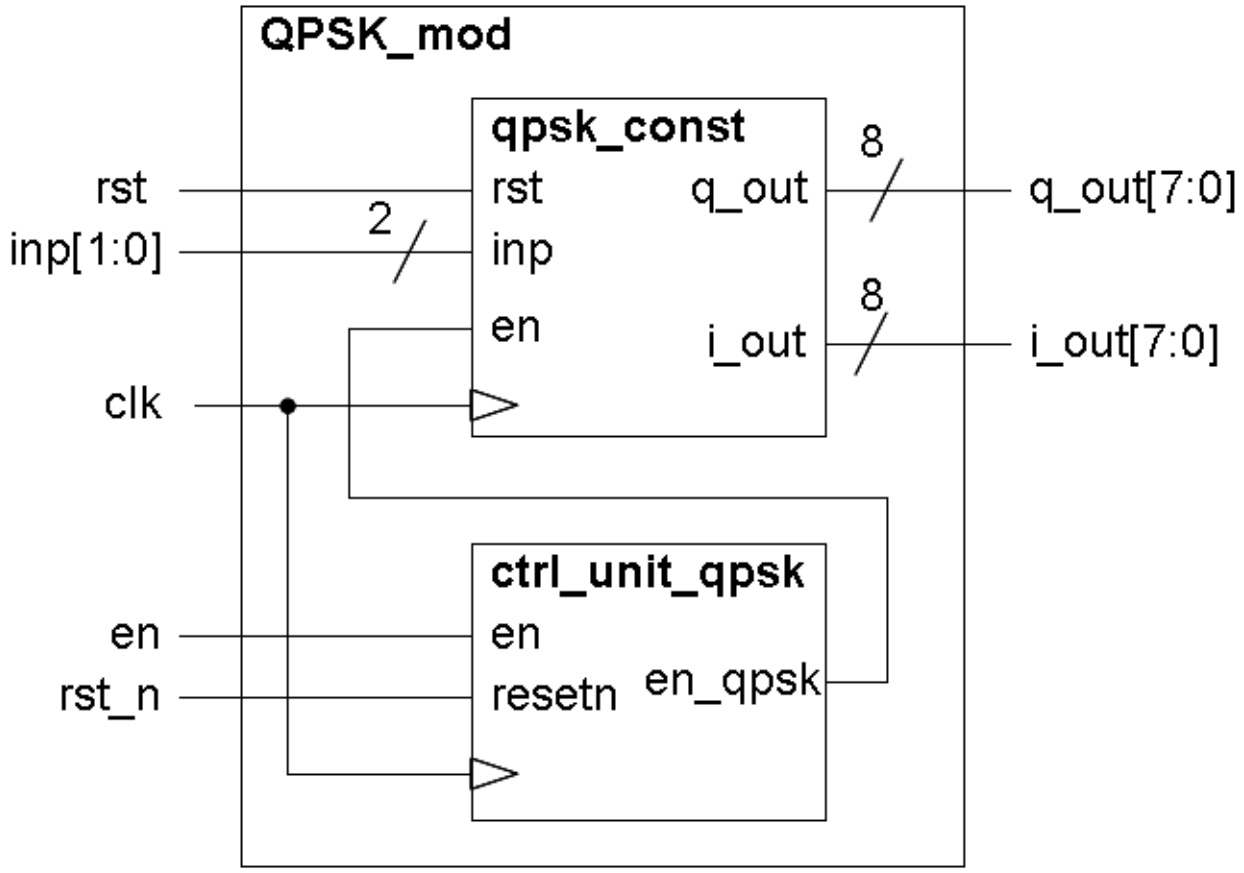


Figure (2.7): Internal part of QPSK_mod

2.4 Multiple Antennas in Wireless System:

A wireless system may be classified in terms of the number of antennas used for transmission and reception. The most traditional configuration uses a single transmit antenna and a single receive antenna, in which case the system is defined as a Single Input Single-Output (SISO) system. With multiple antennas at the receiver, the system is classified as a Single-Input Multiple-Output (SIMO) system. Similarly, with multiple transmit antennas and a single receive antenna, the system is a Multiple-Input Single-Output (MISO) system. Finally, if multiple antennas are employed at both sides of the link, the system is classified as a Multiple-Input Multiple-Output (MIMO) system [3].

2.5 Two Transmit and One Receive Antennas:

The transmission matrix for two transmit antennas is exactly the same as the square matrix for Alamouti scheme except that in the real case, there are no symbol conjugations. Therefore, the transmission matrix is given by:

$$S = \begin{bmatrix} s_1 & s_2 \\ -s_2 & s_1 \end{bmatrix} \tag{2.3}$$

The encoding and decoding here can be constructed in exactly the same way as in the Alamouti's scheme. The receiver receives:

$$\begin{aligned} r_1 &= h_1 s_1 + h_2 s_2 + n_1 \\ r_2 &= -h_1 s_2 + h_2 s_1 + n_2 \end{aligned} \tag{2.4}$$

The combiner combines the received signals as:

$$\begin{aligned} \tilde{s}_1 &= h_1 r_1 + h_2 r_2 \\ \tilde{s}_2 &= h_2 r_1 - h_1 r_2 \end{aligned} \tag{2.5}$$

2.6 Joint Scheme for Two Transmit and Two Receive Antennas:

In this implementation, there are two transmit and two receive antennas. All assumptions in Section 3.2 are followed and applied. The transmitter takes four symbols and constructs two *G2* matrices S1 and S2 . The transmission matrix S1 is used to transmit the pilot sequence and it is equal to the transmission matrix S1 in Equation (2.4). The transmission matrix S1 is used to transmit the user data and it is equal to the transmission matrix S2 in Equation (2.5).At the receiver side, there are two receive antennas, each of which receives four consecutive signals. The first receive antenna receives r1,1 and r 2,1 representing the pilot sequence and then receives r3,1 and r4,1 representing the information data. The second receive antenna receives r1,2 and r 2,2 representing the

pilot sequence and then receives r3,2 and r4,2 representing the information data. The four received signals at the first receive antenna can be written as:

$$R_1 = \begin{bmatrix} r_{1,1} \\ r_{2,1} \end{bmatrix} = S_1 H_1 + N_1 = \begin{bmatrix} s_1 h_1 + s_2 h_2 + n_{1,1} \\ -s_2^* h_1 + s_1^* h_2 + n_{2,1} \end{bmatrix} \quad (2.6)$$

$$R_2 = \begin{bmatrix} r_{3,1} \\ r_{4,1} \end{bmatrix} = S_2 H_1 + N_2 = \begin{bmatrix} s_3 h_1 + s_4 h_2 + n_{3,1} \\ -s_4^* h_1 + s_3^* h_2 + n_{4,1} \end{bmatrix} \quad (2.7)$$

the other four received signals at the second receiver antenna can be written as

$$R_3 = \begin{bmatrix} r_{1,2} \\ r_{2,2} \end{bmatrix} = S_1 H_2 + N_3 = \begin{bmatrix} s_1 h_3 + s_2 h_4 + n_{1,2} \\ -s_2^* h_3 + s_1^* h_4 + n_{2,2} \end{bmatrix} \quad (2.8)$$

$$R_4 = \begin{bmatrix} r_{3,2} \\ r_{4,2} \end{bmatrix} = S_2 H_2 + N_4 = \begin{bmatrix} s_3 h_3 + s_4 h_4 + n_{3,2} \\ -s_4^* h_3 + s_3^* h_4 + n_{4,2} \end{bmatrix} \quad (2.9)$$

After receiving all the transmitted eight signals, the receiver estimate the channel vector from Equation (2.6) and estimates the channel vector from Equation (2.8) as the following:

$$\dot{H}_1 = S_1^{-1} R_1 = \begin{bmatrix} s_1 & s_2 \\ -s_2^* & s_1^* \end{bmatrix}^{-1} \begin{bmatrix} r_{1,1} \\ r_2,1 \end{bmatrix} \quad (2.10)$$

$$\dot{H}_2 = S_1^{-1} R_3 = \begin{bmatrix} s_1 & s_2 \\ -s_2^* & s_1^* \end{bmatrix}^{-1} \begin{bmatrix} r_{1,2} \\ r_{2,2} \end{bmatrix} \quad (2.11)$$

The receiver constructs the channel matrix H1 from Equation (2.10) and constructs the channel matrix H2 from Equation (2.11). The new constructed the channel matrices H1 and H2 can be expressed as in Equation (2.2). After estimating the required channel coefficients vectors, the receiver constructs the vector R1 from the received data vector in Equation (2.7) and constructs the vector R2 from the received data vector in Equation (2.9). The constructed vectors would have the same format as the constructed vector in Equation (2.1). The receiver next uses the constructed matrices H1,H2 and the constructed vectors R1 and R2 for the combining scheme. The combining scheme in this case can be expressed as:

$$\tilde{S}_2 = \ddot{H}_1 \ddot{R}_1 + \ddot{H}_2 \ddot{R}_2 = \begin{bmatrix} \tilde{h}_1^* & \tilde{h}_2 \\ \tilde{h}_2^* & -\tilde{h}_1 \end{bmatrix} \begin{bmatrix} r_{3,1} \\ r_{4,1}^* \end{bmatrix} + \begin{bmatrix} \tilde{h}_3^* & \tilde{h}_4 \\ \tilde{h}_4^* & -\tilde{h}_3 \end{bmatrix} \begin{bmatrix} r_{3,2} \\ r_{4,2}^* \end{bmatrix} \quad (2.12)$$

The combined signals in Equation (2.12) are sent to the maximum-likelihood detector to detect) S2ˆ & S3ˆ (S4 ˆ) . After that, the receiver saves the vector S2 ˆ as S1 and saves the vector R 2as R1 for next iteration. The procedure will go on until all the transmitted data are received and recovered by the receiver.

Chapter Three

VHDL

3.1 Introduction:

VHDL is a hardware description language. It describes the behavior of an electronic circuit or system, from which the physical circuit or system can then be attained(implemented).VHDL stands for VHSIC Hardware Description Language.VHSIC is itself an abbreviation for Very High Speed Integrated Circuits, an initiative funded by the United States Department of Defense in the 1980s that led to the creation of VHDL.

Its first version was VHDL 87, later upgraded to the so-called VHDL 93. VHDL was the original and first hardware description language to be standardized by the Institute of Electrical and Electronics Engineers, through the IEEE 1076 standard.

An additional standard, the IEEE 1164, was later added to introduce a multi-valued logic systemVHDL is intended for circuit synthesis as well as circuit simulation. However, though VHDL is fully simulatable, not all constructs are synthesizable. We will give emphasis to those that are.

A fundamental motivation to use VHDL (or its competitor, Verilog) is that VHDL is a standard, technology/vendor independent language, and is therefore portable and reusable. The two main immediate applications of VHDL are in the field of Programmable Logic Devices (including CPLDs—Complex Programmable Logic Devices and FPGAs—Field Programmable Gate Arrays) and in the field of ASICs (Application Specific Integrated Circuits). Once the VHDL code has been written, it can be used either to implement the circuit in a programmable device (from Altera, Xilinx, Atmel, etc.) or can be submitted to a foundry for fabrication of an ASIC chip. Currently,

many complex commercial chips (microcontrollers, for example) are designed using such an approach. A final note regarding VHDL is that, contrary to regular computer programs which are sequential, its statements are inherently concurrent (parallel). For that reason, VHDL is usually referred to as a code rather than a program. In VHDL,only statements placed inside a PROCESS, FUNCTION, or PROCEDURE are executed sequentially.

3.2 Code Structure:

In this chapter, we describe the fundamental sections that comprise a piece of VHDL code: LIBRARY declarations, ENTITY, and ARCHITECTURE.

3.2.1 Fundamental VHDL Units:

As depicted in figure (2.1), a standalone piece of VHDL code is composed of at least three fundamental sections:

- LIBRARY declarations: Contains a list of all libraries to be used in the design. For example: ieee, std, work, etc.
- ENTITY: Specifies the I/O pins of the circuit.
- ARCHITECTURE: Contains the VHDL code proper, which describes how the circuit should behave (function).

A LIBRARY is a collection of commonly used pieces of code. Placing such pieces inside a library allows them to be reused or shared by other designs.

The typical structure of a library is illustrated in figure(3.1). The code is usually written in the form of FUNCTIONS, PROCEDURES, or COMPONENTS, which are placed inside PACKAGES, and then compiled into the destination library.

The fundamental units of VHDL figure(3.1) will be studied in this chapter.

3.2.2 Library Declarations:

To declare a LIBRARY (that is, to make it visible to the design) two lines of code are needed, one containing the name of the library, and the other a use clause, as shown in the syntax below.

```
LIBRARY library_name;
USE library_name.package_name.package_parts;
```

At least three packages, from three different libraries, are usually needed in a design:

- ieee.std_logic_1164 (from the ieee library),
- standard (from the std library), and
- work (work library).

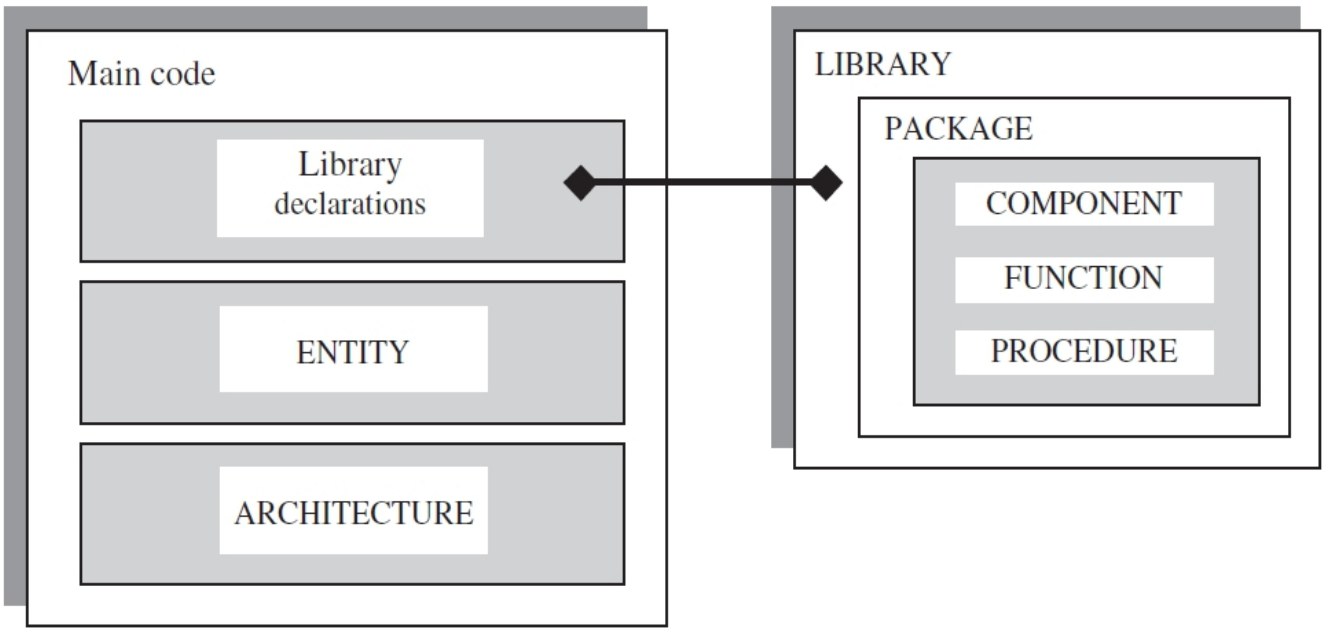


Figure (3.1): Fundamental units of VHDL code

Their declarations are as follows:

```
LIBRARY ieee; -- A semi-colon (;) indicates
USE ieee.std_logic_1164.all; -- the end of a statement or
LIBRARY std; -- declaration, while a double
USE std.standard.all; -- dash (--) indicates a comment.
LIBRARY work;
USE work.all;
```

The libraries std and work shown above are made visible by default, so there is no need to declare them; only the ieee library must be explicitly written. However, the latter is only necessary when the STD_LOGIC (or STD_ULOGIC) data type is employed in the design .

The purpose of the three packages/libraries mentioned above is the following: the std_logic_1164 package of the ieee library specifies a multi-level logic system; std is a resource library (data types, text i/o, etc.) for the VHDL design environment; and the work library is where we save our design (the .vhd file, plus all files created by the compiler, simulator, etc.).

Indeed, the ieee library contains several packages, including the following:

- std_logic_1164: Specifies the STD_LOGIC (8 levels) and STD_ULOGIC (9 levels)multi-valued logic systems.
- std_logic_arith: Specifies the SIGNED and UNSIGNED data types and related arithmetic and comparison operations. It also contains several data conversion functions, which allow one type to be converted into another: conv_integer(p), conv_unsigned(p, b), conv_signed(p, b), conv_std_logic_vector(p, b).

- ❖ std_logic_signed: Contains functions that allow operations with STD_LOGIC_VECTOR data to be performed as if the data were of type SIGNED.
- ❖ std_logic_unsigned: Contains functions that allow operations with STD_LOGIC_VECTOR data to be performed as if the data were of type UNSIGNED.

3.2.3 ENTITY:

An ENTITY is a list with specifications of all input and output pins (PORTS) of the circuit. Its syntax is shown below.

Code Structure 15

```
ENTITY entity_name IS
PORT (
port_name : signal_mode signal_type;
port_name : signal_mode signal_type;
...);
END entity_name;
```

The mode of the signal can be IN, OUT, INOUT, or BUFFER. As illustrated in figure (3.2), IN and OUT are truly unidirectional pins, while INOUT is bidirectional.

BUFFER, on the other hand, is employed when the output signal must be used (read) internally.

The type of the signal can be BIT, STD_LOGIC, INTEGER, etc.

Finally, the name of the entity can be basically any name, except VHDL reserved words .

Example: Let us consider the NAND gate of figure (3.3). Its ENTITY can be specified as:

```
ENTITY nand_gate IS
PORT (a, b : IN BIT;
x : OUT BIT);
END nand_gate;
```

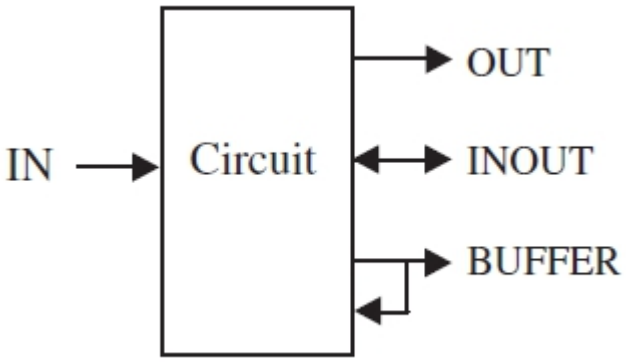


Figure (3.2): Signal modes

Figure (3.3): NAND gate

The meaning of the ENTITY above is the following: the circuit has three I/O pins ,being two inputs (a and b, mode IN) and one output (x, mode OUT). All three signals are of type BIT. The name chosen for the entity was nand_gate.

3.2.4 ARCHITECTURE:

The ARCHITECTURE is a description of how the circuit should behave (function).
Its syntax is the following:

```
ARCHITECTURE architecture_name OF entity_name IS
[declarations]
BEGIN
(code)
END architecture_name;
```

As shown above, an architecture has two parts: a declarative part (optional), where signals and constants (among others) are declared, and the code part (from BEGIN down). Like in the case of an entity, the name of an architecture can be basically any name (except VHDL reserved words), including the same name as the entity's.

Example: Let us consider the NAND gate of figure (3.3) once again.

```
ARCHITECTURE myarch OF nand_gate IS
BEGIN
x <= a NAND b;
END myarch;
```

The meaning of the ARCHITECTURE above is the following: the circuit must perform the NAND operation between the two input signals (a, b) and assign (''<¼'')the result to the output pin (x). The name chosen for this architecture was myarch.
In this example, there is no declarative part, and the code contains just a single assignment.

3.3 Design implementation using Xilinx ISE:

Web PACK ISE design software offers a complete design suite based on the Xilinx ISE series software. Individual Web PACK ISE modules give us the ability to the design environment to our chosen PLDs as well as the preferred design flow [28].

In general, the design flow for FPGAs and CPLDs is identical. Can be choose whether to enter the design in schematic form or in HDL, such as VHDL, Verilog. The design can also comprise of a mixture of schematic diagrams and embedded HDL symbols. There is also a facility to create state machines [28].

Xilinx Integrated Software Environment (ISE) is a powerful yet flexible integrated design environment that allows designing Xilinx FPGA devices from start to finish. ISE as shown in Figure (3.4) [13], includes design entry, synthesis and implementation tools delivering the industry's fastest place and route times, highest performance, and most advanced design methodologies. ISE controls all aspects of the design flow.

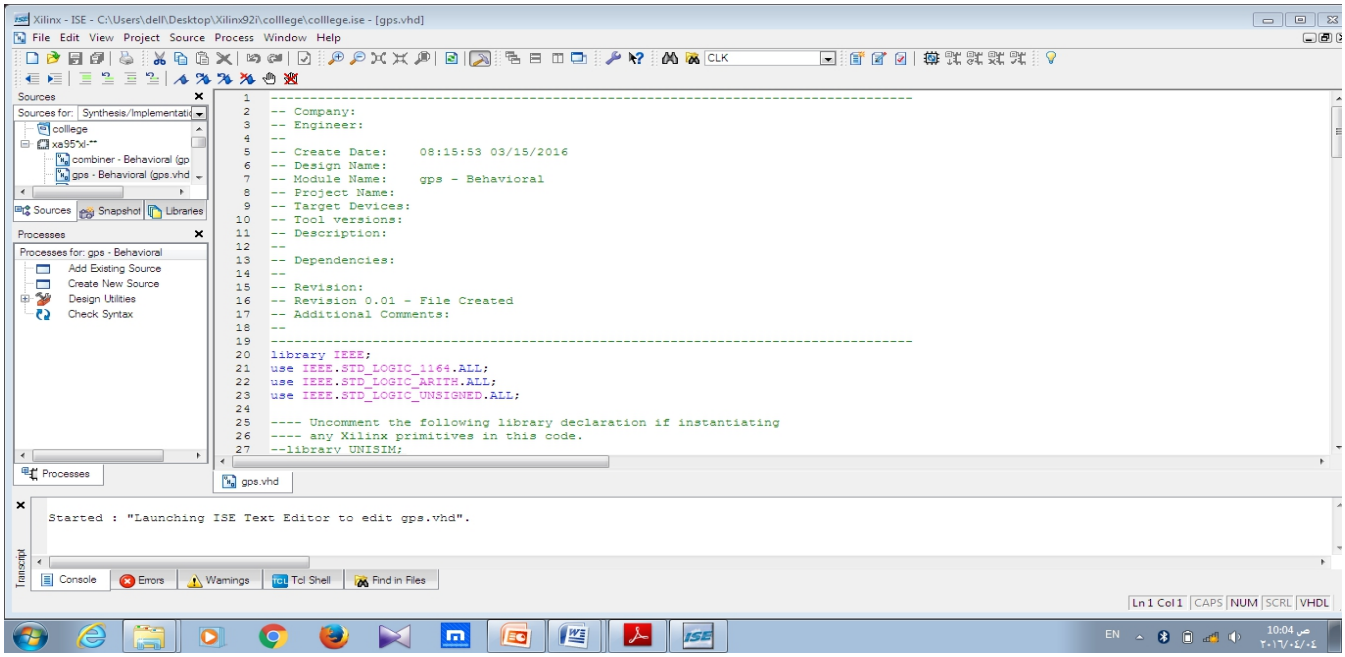


Figure (3.4): Xilinx integrated software environment

Through the Project Navigator interface, all of the design entry and design implementation tools can be accessed. Design implementation is the process of translating, mapping, placing, routing, and generating a BIT file for your design. The Design Implementation tools are embedded in the ISE software for easy access and project management. Design implementation tools, and must incorporate placement constraints through a User Constraints File (UCF).

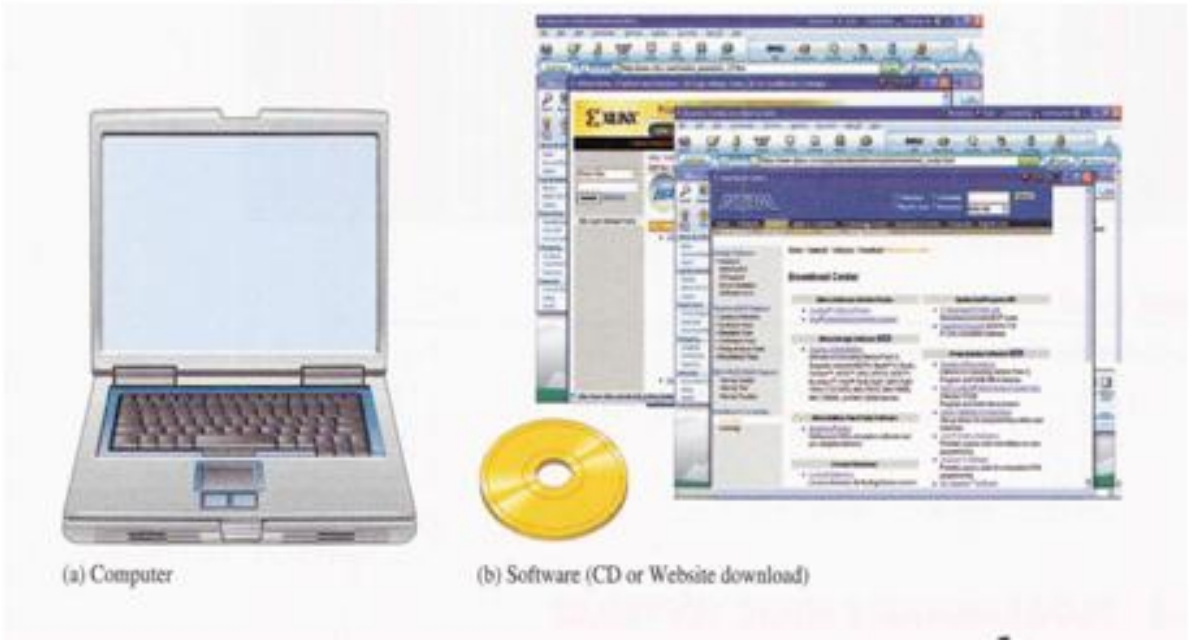


Figure (3.5): Essential elements for programming

Chapter Four

Work and Result

4.1 Programming and Simulation:

In this chapter we will writ code for each block of the transmitter shown in figure(4.1) by using VHDL language and implemented by Xilinx ISE 9.2 shown in figure(4.2) to get on results.

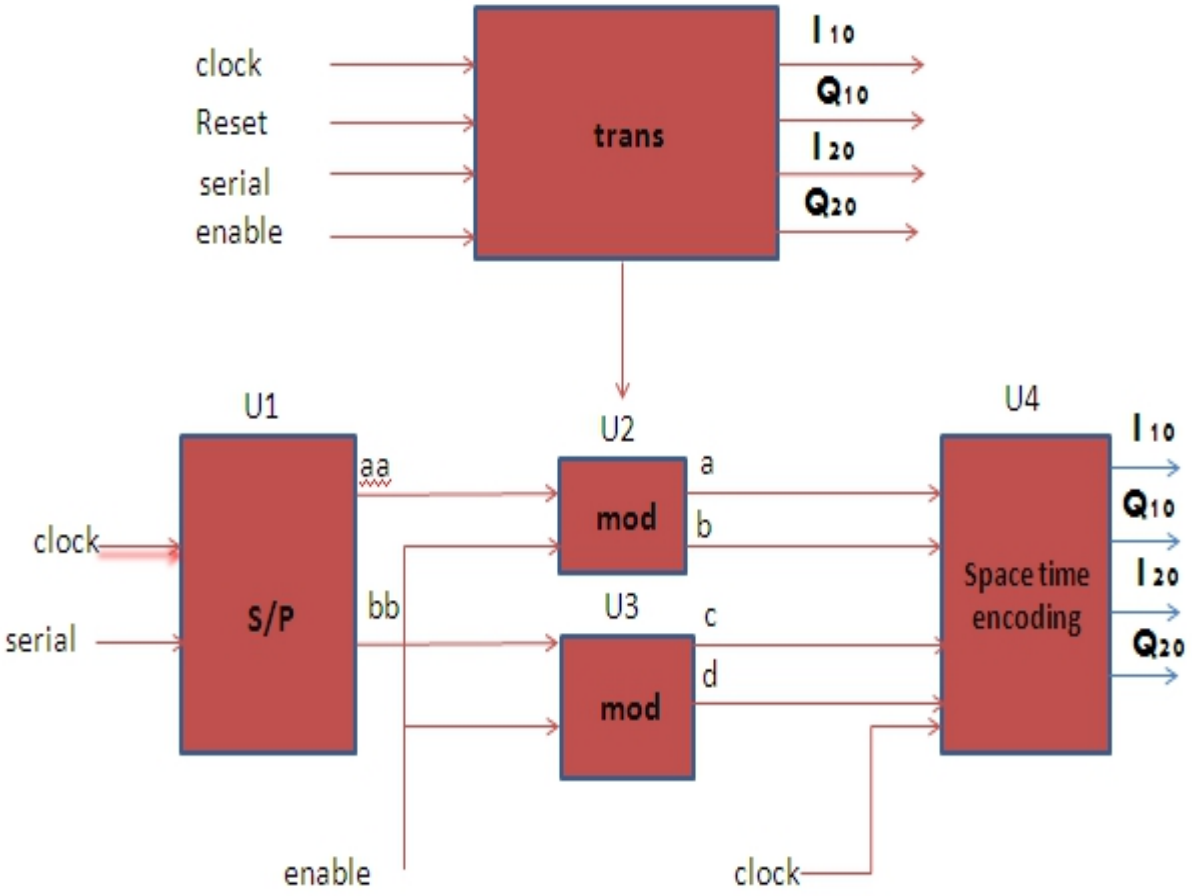
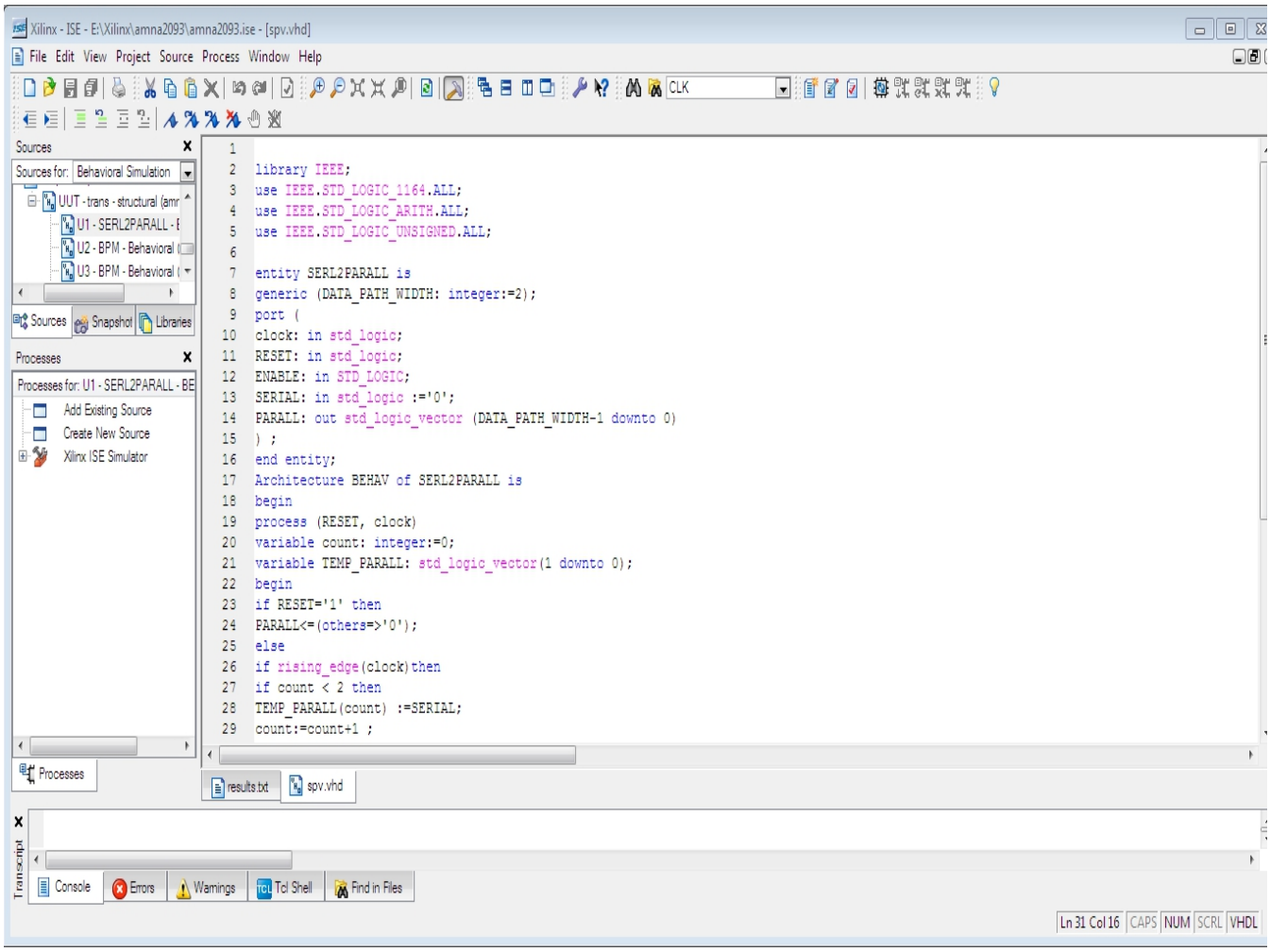


Figure (4.1): Transmitter block diagram



Figure(4.2): Xilinx ISE 9.2

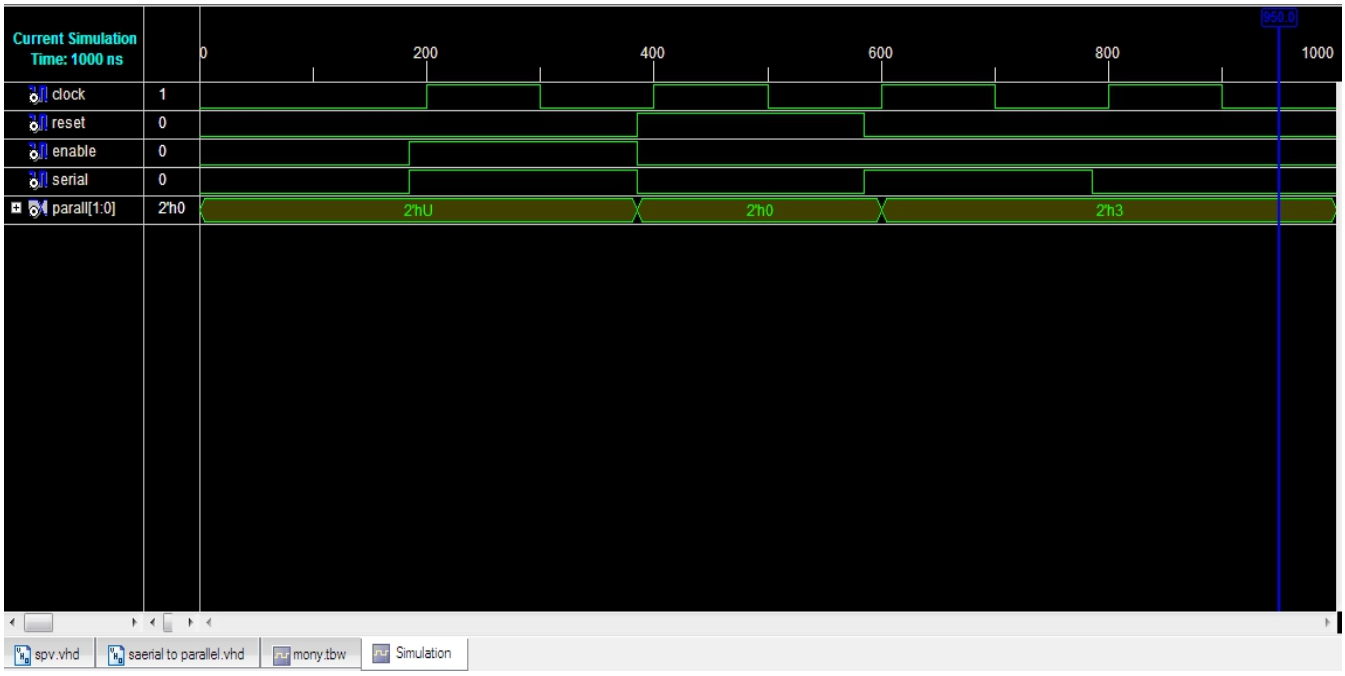
4.2 The VHDL code of the Serial to parallel block:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
```

```
entity SERL2PARALL is
generic (DATA_PATH_WIDTH: integer:=2);
port (
clock: in std_logic;
RESET: in std_logic;
ENABLE: in STD_LOGIC;
SERIAL: in std_logic :='0';
PARALL: out std_logic_vector (DATA_PATH_WIDTH-1 downto 0)
) ;
end entity;
Architecture BEHAV of SERL2PARALL is
begin
process (RESET, clock)
variable count: integer:=0;
variable TEMP_PARALL: std_logic_vector(1 downto 0);
begin
if RESET='1' then
PARALL<=(others=>'0');
else
if rising_edge(clock)then
if count < 2 then
TEMP_PARALL(count) :=SERIAL;
count:=count+1 ;
```

```
end if ;
if count=2 then
count:= 0;
if count= 0 then
PARALL<=TEMP_PARALL;
end if;
end if ;
end if;
end if;
end process;
end BEHAV;
```

4.3 Simulation of the serial to parallel block:

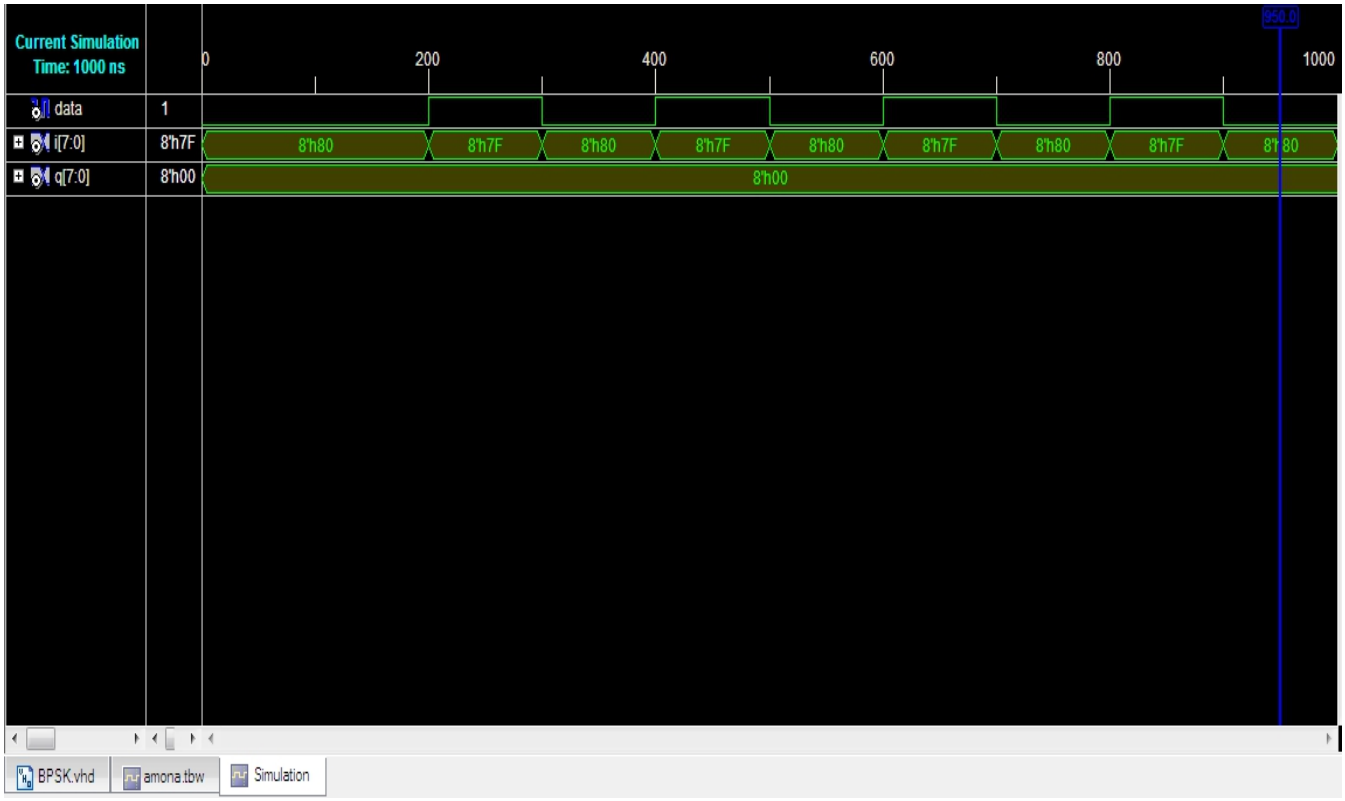


Figure(4.3): Simulation of the serial to parallel block

4.4 The VHDL code of the mod(QPSK) block:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;




entity BPM is
    Port ( DATA : in  STD_LOGIC;
           I : out  SIGNED(7 downto 0);
           Q : out      SIGNED(7 downto 0));
end BPM;

architecture Behavioral of BPM is

begin
WITH DATA SELECT I<=
   "01111111"WHEN '1',
"10000000" WHEN OTHERS;
Q<="00000000";
end Behavioral;
```

4.5 Simulation of the mod(QPSK) block:



Figure(4.4): Simulation of the mod(QPSK) block

4.6 The VHDL code of the space time encoding block:

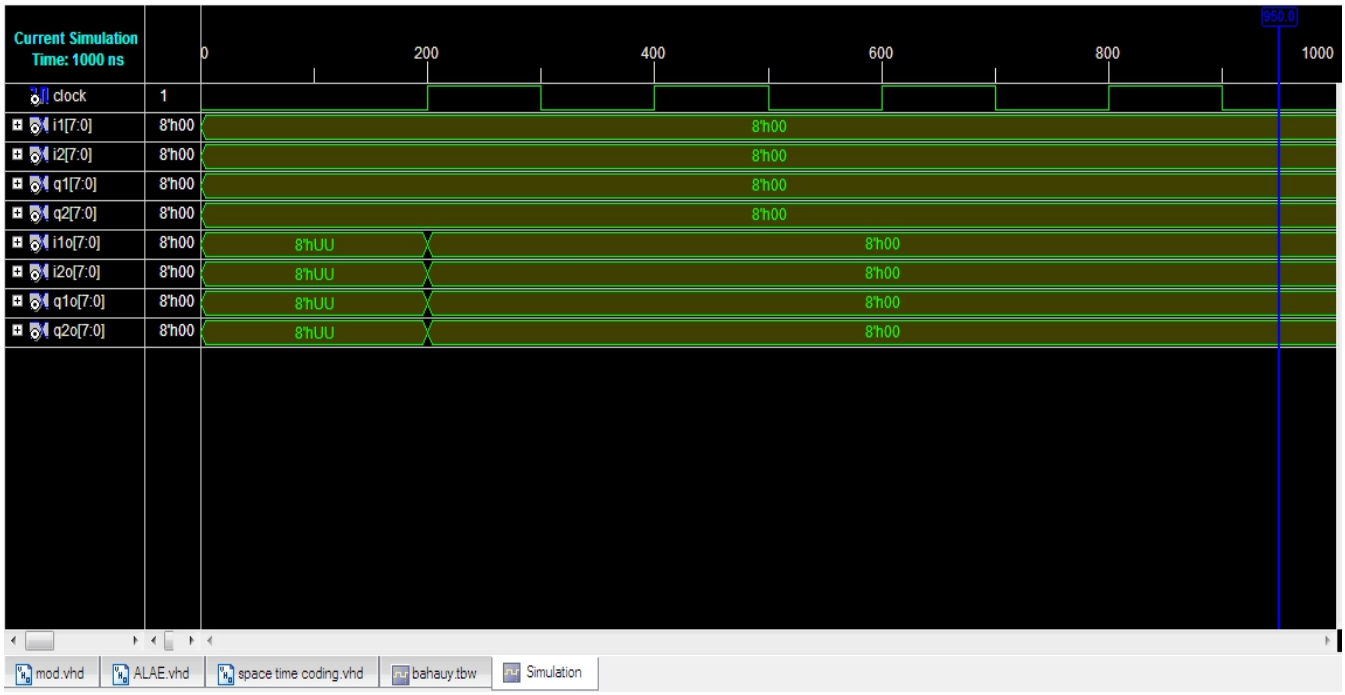
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;



entity ALAE is
```

```
    Port ( CLOCK  : in  STD_LOGIC;
           I1 : in  SIGNED (7 downto 0);
           I2 : in  SIGNED (7 downto 0);
           Q1 : in  SIGNED (7 downto 0);
           Q2 : in  SIGNED (7 downto 0);
           ------------------------
           I1O : out  SIGNED (7 downto 0);
           I2O : out  SIGNED (7 downto 0);
           Q1O : out  SIGNED (7 downto 0);
           Q2O : out  SIGNED (7 downto 0));
            -----------done : out std_logic);
end ALAE;

architecture Behavioral of ALAE is
SIGNAL TMP1I,TMP1Q :SIGNED(7 DOWNTO 0);--ANTENNA1 VARIABLE
SIGNAL TMP2I,TMP2Q :SIGNED(7 DOWNTO 0);--ANTENNA2 VARIABLE
SIGNAL STATE :STD_LOGIC;
---------signal done_i : std_logic;
begin
  PROCESS(CLOCK )
       BEGIN
 IF (CLOCK ' EVENT AND CLOCK  ='1') THEN
        IF(STATE ='0') THEN--FIRST CYCLE
```

```
----- done_i <= '0';
            TMP1I <= I1;
            TMP1Q <= Q1;

            TMP2I <= I2;
            TMP2Q <= Q2;
            ----------done_i <= '0';
           STATE <= '1';

          ELSE
            TMP1I <= -I2;
            TMP1Q <= Q2;

            TMP2I <= I1;
            TMP2Q <= -Q1;
             --------- done_i <= '1';
            STATE <='0';

          END IF;
       END IF;

   END PROCESS;
   I1O <= TMP1I ;
```

```
Q1O <= TMP1Q ;

I2O <= TMP2I ;
Q2O <= TMP2Q ;
----------done <= done_i;

end Behavioral;
```

4.7 Simulation of the space time encoding block:



Figure(4.5): Simulation of the space time encoding block

4.8 The VHDL code of the transmitter block:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;


 ----------------------------------
 ENTITY trans IS
 PORT (clock : IN STD_LOGIC;
RESET: in std_logic;
ENABLE: in STD_LOGIC;
SERIAL: in std_logic :='0';
 I1O : out  SIGNED (7 downto 0);
  Q1O : out  SIGNED(7 downto 0);
  I2O : out  SIGNED (7 downto 0);
Q2O : out  SIGNED(7 downto 0));
----------done_tx : out std_logic);
 END trans;
 ---------------------------------
 ARCHITECTURE structural OF trans IS


 COMPONENT SERL2PARALL IS
```

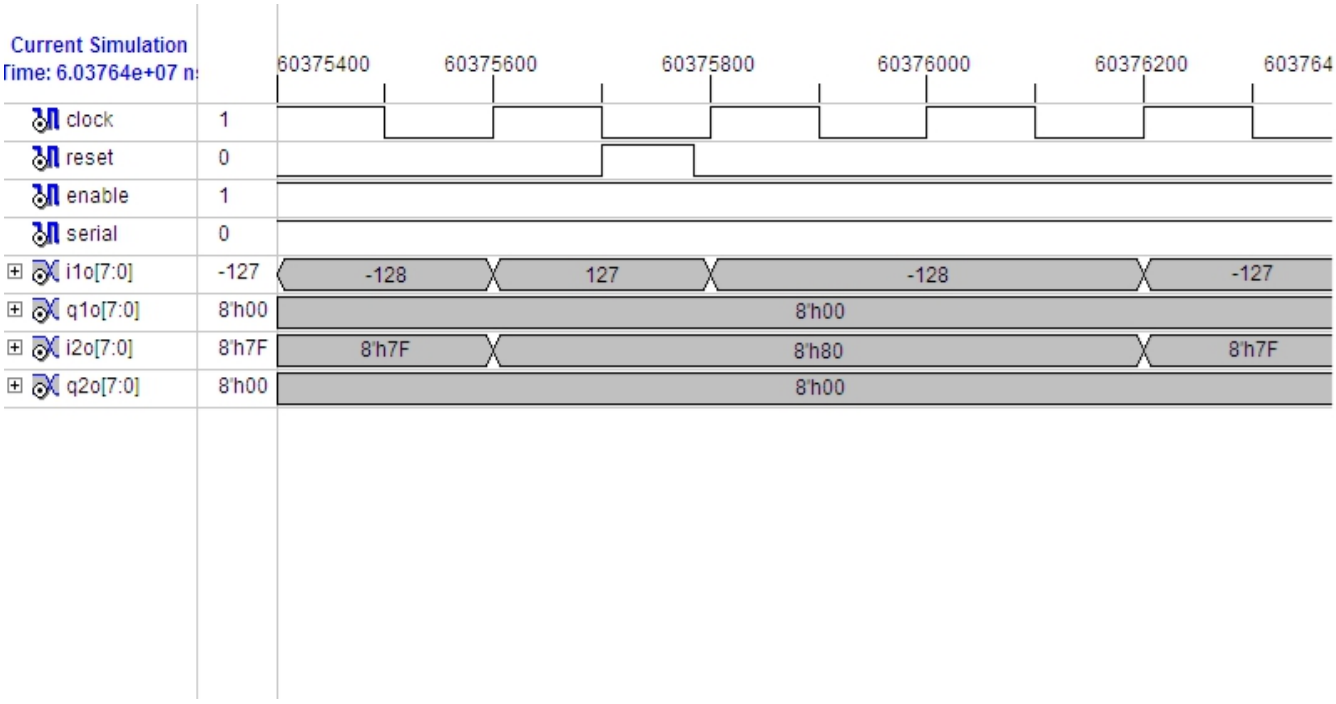
```
 PORT (
clock : in std_logic;
RESET: in std_logic;
ENABLE: in STD_LOGIC;
SERIAL: in std_logic :='0';
PARALL: out std_logic_vector (1 downto 0)
) ;
 END COMPONENT;
 -------------
 COMPONENT BPM  IS
 Port ( DATA : in  STD_LOGIC;
          I : out     SIGNED(7 downto 0);
          Q : out     SIGNED(7 downto 0));
 END COMPONENT;
 -------------

  COMPONENT ALAE IS
  Port ( clock  : in  STD_LOGIC;
          I1 : in  SIGNED(7 downto 0);
          Q1: in SIGNED(7 downto 0);
          I2 : in  SIGNED(7 downto 0);
          Q2 : in SIGNED(7 downto 0);
           ----------------------------
```

```
        I1O : out  SIGNED(7 downto 0);
        Q1O : out  SIGNED(7 downto 0);
        --------------------
        I2O : out  SIGNED(7 downto 0);
        Q2O : out  SIGNED(7 downto 0));
         ----------done_tx : out std_logic);
END COMPONENT;
-----------------------------

SIGNAL PARALL: std_logic_vector(1 downto 0);
SIGNAL aa,bb: STD_LOGIC;
SIGNAL a: SIGNED(7 downto 0);
SIGNAL b:  SIGNED(7 downto 0);
SIGNAL c: SIGNED(7 downto 0);
SIGNAL d: SIGNED(7 downto 0);

BEGIN

aa<=PARALL(0);   bb<=PARALL(1);

U1: SERL2PARALL PORT MAP (clock ,RESET,ENABLE,SERIAL, PARALL);
U2: BPM  PORT MAP (aa, a,b);
U3: BPM  PORT MAP (bb, c,d);
```

```
U4: ALAE  PORT MAP ( clock , a,b,c,d, I1O, Q1O, I2O, Q2O  );
```

```
END structural;
```

4.9 Simulation of the transmitter block:



Figure(4.6): Simulation of the transmitter block

Chapter Five

Conclusion and Future Work

5.1 Conclusion:

1.We can use verilog to design the system .

2.We can design this with more than two system ,so we can use 4-antenna or 8-antenna.

3.This system can be completed by design MIMO with OFDM.

5.2 Future Work :

For future work, there are some possible extensions to the presented work as follows:

1. The scheme may be generalized for two transmit antennas and M receiver antennas with small computation complexity, or increasing the number of transmitter to make it equal to the received antenna
2. The proposed design can be extended by using a higher order constellation such as 16 QAM
3. The design can be investigated by using different modulation techniques, such as OFDM, when it is used in conjunction with space-time coding.
4. It can be extended by using a error detection and error correction using (VHDL) language.
5. The proposed design can be implemented using fiber optical as transmission medium.

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